## WHAT IS CLAIMED IS:

- 1. A semiconductor memory device comprising:
- 2 a plurality of word lines each extending in a first
- 3 direction;
- 4 aplurality of bit lines each extending in a second direction
- 5 crossing said first direction;
- 6 a straight active region extending in a direction different
- 7 from said first and second directions, said active region
- 8 crossing three or more word lines and three or more bit lines;
- 9 and
- 10 a plurality of memory cells formed in said active regions.
  - 1 2. The device as claimed in claim 1, wherein each said memory
- 2 cell includes a data storage capacitor, a first switching element
- 3 connected to said data storage capacitor, and a second switching
- 4 element connected to said data storage capacitor.
- 3. The device as claimed in claim 2, said device further
- 2 comprising:
- 3 a capacitor contact connected to the data storage capacitor
- 4 and formed on said active region between the adjacent first and
- 5 second word lines;
- a first bit line contact connected to a first one of said
- 7 bit lines and arranged such that said first word line is sandwiched
- 8 between said capacitor contact and said first bit line contact;
- 9 and
- 10 a second bit line contact connected to a second one of said

- 11 bit lines and arranged such that said second word line is
- 12 sandwiched between said capacitor contact and said second bit
- 13 line contact.
  - 1 4. The device as claimed in claim 1, wherein said active
  - 2 region substantially extends from end to end of a memory cell
  - 3 array area.
- 5. The device as claimed in claim 1, said device further
- 2 comprising:
- 3 a plurality of bit line contacts each connected to a single
- 4 bit line, there being four word lines between the adjacent bit
- 5 line contacts.
- 1 6. The device as claimed in claim 2, said device further
- 2 comprising:
- a first row decoder driving a first set of said word lines,
- 4 said first set coupled to said first switching elements;
- 5 a second row decoder driving a second set of said word lines,
- 6 said second set coupled to said second switching elements, said
- 7 second row decoder receiving a row address signal;
- 8 a first column decoder selecting a first group of said bit
- 9 lines, said first group coupled to said first switching elements;
- 10 and
- 11 a second column decoder selecting a second group of said
- 12 bit lines, said second group coupled to said second switching
- 13 elements, said second column decoder receiving a portion of said
- 14 row address signal.

- 7. The device as claimed in claim 6, wherein
- 2 when said second row decoder drives said second set of said

28

- 3 word lines based on one of incrementing and decrementing of said
- 4 row address signals, said second column decoder alternatively
- 5 selects the bit lines adjacent to each other among said second
- 6 group.
- 8. The device as claimed in claim 2, said device further
- 2 comprising:
- 3 a first row decoder driving a first set of said word lines,
- 4 said first set coupled to said first switching elements, said
- 5 first row decoder being activated when data access is performed
- 6 to a selected memory cell;
- 7 a second row decoder driving a second set of said word lines,
- 8 said second set coupled to said second switching elements, said
- 9 second decoder receiving a refresh address signal;
- 10 a first column decoder selecting a first group of said bit
- 11 lines, said first group coupled to said first switching elements;
- 12 and
- a sense amplifier circuit sensing a second group of said
- 14 bit lines, said second group coupled to said second switching
- 15 element, said sense amplifier circuit being controlled by a sense
- 16 enable signal and not controlled by an address signal.
- 9. A semiconductor memory device comprising:
- 2 a plurality of word lines;
- 3 a plurality of bit lines;

- 4 an active region formed on a semiconductor substrate and
- 5 defined by an element separation region, a boundary between said
- 6 active region and said element separation region being
- 7 substantially straight between at least three adjacent word
- 8 lines; and
- 9 a plurality of memory cells formed on a semiconductor
- 10 substrate.
  - 1 10. The device as claimed in claim 9, wherein each said
  - 2 memory cell includes a data storage capacitor, a first switching
  - 3 element connected to the data storage capacitor, and a second
- 4 switching element connected to the data storage capacitor, each
- 5 of said memory cells connected to a corresponding one of said
- 6 word lines and a corresponding one of said bit lines.
- 1 11. The device as claimed in claim 10, said device further
- 2 comprising:
- 3 a capacitor contact connected to the data storage capacitor
- 4 and formed on said active region between the adjacent first and
- 5 second word lines;
- a first bit line contact connected to a first one of said
- 7 bit lines and arranged such that said first word line is sandwiched
- 8 between said capacitor contact and said first bit line; and
- 9 a second bit line contact connected to a second one of said
- 10 bit lines and arranged such that said second word line is
- 11 sandwiched between said capacitor contact and said second bit
- 12 line.

- 1 12. The device as claimed in claim 9, wherein said active
- 2 region substantially extends from end to end of a memory cell
- 3 array area.
- 1 13. The device as claimed in claim 9, said device further
- 2 comprising:
- 3 a plurality of bit line contacts each connected to a single
- 4 bit line, there being four word lines between the adjacent bit
- 5 line contacts.
- 1 14. The device as claimed in claim 9, said device further
- 2 comprising:
- 3 a first row decoder driving a first set of said word lines,
- 4 said first set coupled to said first switching elements;
- 5 a second row decoder driving a second set of said word lines,
- 6 said second set coupled to said second switching elements, said
- 7 second row decoder receiving a row address signal;
- 8 a first column decoder selecting a first group of said bit
- 9 lines, said first group coupled to said first switching elements;
- 10 and
- 11 a second column decoder selecting a second group of said
- 12 bit lines, said second group coupled to said second switching
- 13 elements, said second column decoder receiving a portion of said
- 14 row address signal.
  - 1 15. The device as claimed in claim 14, wherein
  - 2 when said second row decoder drives said second set of said
  - 3 word lines based on one of incrementing and decrementing of said

- 4 row address signals, said second column decoder alternatively
- 5 selects the bit lines adjacent to each other among said second
- 6 group.
- 1 16. The device as claimed in claim 9, said device further
- 2 comprising:
- 3 a first row decoder driving a first set of said word lines,
- 4 said first set coupled to said first switching elements, said
- 5 first row decoder being activated when data access is performed
- 6 to a selected memory cell;
- 7 a second row decoder driving a second set of said word lines,
- 8 said second set coupled to said second switching elements, said
- 9 second decoder receiving a refresh address signal;
- 10 a first column decoder selecting a first group of said bit
- 11 lines, said first group coupled to said first switching elements;
- 12 and
- a sense amplifier circuit sensing a second group of said
- 14 bit lines, said second group coupled to said second switching
- 15 element, said sense amplifier circuit being controlled by a sense
- 16 enable signal and not controlled by an address signal.
  - 1 17. A semiconductor memory device comprising:
- a first row decoder driving at least first and second word
- 3 lines;
- a second row decoder driving at least third and fourth word
- 5 line;
- 6 first, second and third bit lines;
- 7 a first memory cell having a first capacitor, a first

- 8 switching element coupled between said first capacitor and said
- 9 first bit line and coupled to said first word line, and a second
- 10 switching element coupled between said first capacitor and said
- 11 second bit line and coupled to said third word line; and
- 12 a second memory cell having a second capacitor, a first
- 13 switching element coupled between said second capacitor and said
- 14 first bit line and coupled to said second word line, and a second
- 15 switching element coupled between said second capacitor and said
- 16 third bit line and coupled to said fourth word line.
  - 1 18. The device as claimed in claim 17, said device further
  - 2 comprising:
  - 3 a first column decoder selecting at least said first bit
  - 4 line;
- 5 a second column decoder selecting at least said second and
- 6 third bit lines, said second column decoder receiving a portion
- 7 of a row address signal.
- 1 19. The device as claimed in claim 17, said device further
- 2 comprising:
- 3 a first sense amplifier coupled to said first bit line and
- 4 controlled by a first sense enable signal;
- 5 a second sense amplifier coupled to said second bit line
- 6 and controlled by a second sense enable signal; and
- 7 a third sense amplifier coupled to said third bit line and
- 8 controlled by said second sense enable signal.
- 1 20. The device as claimed in claim 19, wherein said second

- 2 and third sense amplifiers are not controlled by a row address
- 3 signal.
- 1 21. The device as claimed in claim 17, wherein said first
- 2 and second memory cells are formed on an active region which
- 3 are designed in an elongate shape, an edge of said active region
- 4 does not have a bent portion between said first and second memory
- 5 cells.
- 1 22. The device as claimed in 21, wherein each of said first
- 2 to fourth word lines extends in a first direction, each of said
- 3 first to third bit lines extends in a second direction, said
- 4 active region extends in a third direction different from said
- 5 first and second directions.